

ISTANBUL TECHNICAL

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UNIVERSITY

COMPUTER ENGINEERING

DIGITAL CIRCUITS LABORATORY

EXPERIMENT REPORT

EXPERIMENT NO: 2

EXPERIMENT NAME: Combinational Circuits

EXPERIMENT DATE: 07.03.2014

GROUP NO: B10

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1. **Aim :**

In this experiment, our aim is that to find the lowest cost expressions for combinational logic circuits and to create these expressions with different methods.

1. **Experiments :**

**Experiment 1:**

F(A,B,C,D)=∑1(0,3,5,7,11,12,13) + ∑Q(1,8,15)

**Truth Table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **F** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | Q |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | Q |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | Q |

**Karnaugh Diagram**

**CD 00 01 11 10**

|  |  |  |  |
| --- | --- | --- | --- |
| **1** | **Q** | **1** | **0** |
| **0** | **1** | **1** | **0** |
| **1** | **1** | **Q** | **0** |
| **Q** | **0** | **1** | **0** |

**AB**

**00**

**01**

**11**

**10**

All prime implicants: A’D , CD , ABC’ , A’B’C’ , BD , AC’D’, B’C’D’

We find function of F via Karnaugh Diagram and Quine-McCluskey Method as

F = (ABC’+A’B’C’+BD+CD).

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As drawn above, we got results correctly which is expected to be true.

F(1),F(8) and F(15) ,which are uncertain inputs are obtained as 1, 0 and 1 respectively. The reason for this is directly related to circuit elements used. Function values are as follows:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **F** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**Experiment 2:**

The function of F in the previous experiment was created again using with only NAND and NOT gates.



F = (ABC’+A’B’C’+BD+CD)

As drawn above, we made it real by using TVE gates and got the correct results.1. and 2. Experiments ended up with the same results.

**Experiment 3:**

The function of F in the previous experiment was created again using with 8:1 multiplexer and NOT gates.



This experiment is same the Experiment 2. Thus, all of results in the previous are valid for it.

**Experiment 4:**



To solve F1 = A’C’+BC equations, we used Consensus Theorem so that it turns F1 = A’BC’+ A’B’C’+ABC+A’BC.

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **C** | **F1** |
| **0** | **0** | **0** | **1** |
| **0** | **0** | **1** | **0** |
| **0** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** |



To solve F2 = A’B’C’+AB equations, we used Consensus Theorem so that it turns F2 = A’B’C’+ABC+ABC’.

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **C** | **F2** |
| **0** | **0** | **0** | **1** |
| **0** | **0** | **1** | **0** |
| **0** | **1** | **0** | **0** |
| **0** | **1** | **1** | **0** |
| **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** |

Both theoretical and practical values for F1 and F2 functions are same.

**Questions:**

**3)** F’(A,B,C,D) = A’B’C+AC’D’+BD’

If we apply De Morgan Rules, this equation turns PoS form. (Product of Sum).

F (A,B,C,D) = (A+B+C’)(A’+C+D)(B’+D)



**4)** 2:4 Decoder was created using with only NAND gates.

